Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the above-identified application.

Listing of Claims:

1. (**Previously Presented**) A method of packet processing comprising:

parsing a packet using a first peripheral processor, said packet having a header portion, to determine a vector;

coordinating processing using said vector;

deconstructing said packet header to form header data using a second peripheral processor;

searching one or more data structures based on said header data to produce search results using a third peripheral processor;

editing said packet based on said search results, said header data, and said vector using a fourth peripheral processor;

wherein said coordinating comprises,

storing data within a shared register set coupled to each of said peripheral processors,

sharing said data with said parsing, said deconstructing, said searching, and said editing, and

monitoring said deconstructing, said searching, and said editing.

2. (**Canceled**)

3. (**Original**) The method of Claim 1, further comprising buffering said packet before said parsing.

4. (**Original**) The method of Claim 1, wherein:

said deconstructing further comprises forming a search argument; and

said searching uses said search argument.

5. **(Currently Amended)** A ~~The~~ method of packet processing comprising ~~of Claim 1, wherein~~:

parsing a packet using a first peripheral processor, said packet having a header portion, to determine a vector;

coordinating processing using said vector;

deconstructing said packet header to form header data using a second peripheral processor;

searching one or more data structures based on said header data to produce search results using a third peripheral processor; and

editing said packet based on said search results, said header data, and said vector using a fourth peripheral processor; wherein

said deconstructing ~~further~~ comprises forming a search argument, [[;]]

said coordinating ~~further~~ comprises,

storing data within a shared register set coupled to each of said peripheral processors,

sharing said data with said parsing, said deconstructing, said searching, and said editing,

monitoring said deconstructing, said searching, and said editing, and

operating on said search argument to form a modified search argument prior to said searching, [[;]] and

said searching uses said modified search argument.

6. **(Previously presented)** An apparatus for packet processing, comprising:

one or more peripheral processors to perform one or more packet processing tasks, wherein said one or more peripheral processors comprises,

a packet parser to determine a vector;

a central processor to coordinate said one or more packet processing tasks using said vector; and

a shared register set coupled to said one or more peripheral processors and to said central processor; wherein,

said central processor and said one or more peripheral processors share data using said shared register set.

7. **(Original)** The apparatus of Claim 6, wherein said central processor comprises a general purpose processor.

8. **(Original)** The apparatus of Claim 6, wherein said central processor comprises a microsequencer.

9. **(Original)** The apparatus of Claim 6, wherein said central processor comprises more than one processor acting in concert.

10. **(Original)** The apparatus of Claim 6, wherein one or more of said peripheral processors comprise fixed logic circuits.

11. **(Original)** The apparatus of Claim 6, wherein one or more of said peripheral processors comprise programmable logic circuits.

12. **(Original)** The apparatus of Claim 6, wherein one or more of said peripheral processors comprise a programmable state machine.

13. **(Canceled)**

14. **(Original)** The apparatus of Claim 6, wherein said central processor and at least one peripheral processor together form at least a part of a single application specific integrated circuit.

15. **(Previously presented)** A computer system for packet processing, comprising computer instructions for:

parsing a packet using a first peripheral processor, said packet having a header portion, to determine a vector;

coordinating processing using said vector;

deconstructing said packet header to form header data using a second peripheral processor;

searching one or more data structures based on said header data to produce search results using a third peripheral processor;

editing said packet based on said search results, said header data, and said vector using a fourth peripheral processor;

wherein said coordinating comprises,

storing data within a shared register set coupled to each of said peripheral processors,

sharing said data with said parsing, said deconstructing, said searching, and said editing, and

monitoring said deconstructing, said searching, and said editing.

16. **(Canceled)**

17. **(Original)** The computer system of Claim 15, further comprising buffering said packet before said parsing.

18. **(Original)** The computer system of Claim 15, wherein:

said deconstructing further comprises forming a search argument; and

said searching uses said search argument.

19. **(Currently Amended)** A ~~The~~ computer system for packet processing, comprising computer instructions for ~~of Claim 15, wherein~~:

parsing a packet using a first peripheral processor, said packet having a header portion, to determine a vector;

coordinating processing using said vector;

deconstructing said packet header to form header data using a second peripheral processor;

searching one or more data structures based on said header data to produce search results using a third peripheral processor; and

editing said packet based on said search results, said header data, and said vector using a fourth peripheral processor; wherein

said deconstructing ~~further~~ comprises forming a search argument,[[;]]

said coordinating ~~further~~ comprises,

storing data within a shared register set coupled to each of said peripheral processors,

sharing said data with said parsing, said deconstructing, said searching, and said editing,

monitoring said deconstructing, said searching, and said editing and

operating on said search argument to form a modified search argument prior to said searching, [[;]]and

said searching uses said modified search argument.

20. **(Previously Presented)** A computer-readable storage medium, comprising computer instructions for:

parsing a packet using a first peripheral processor, said packet having a header portion, to determine a vector;

coordinating processing using said vector;

deconstructing said packet header to form header data using a second peripheral processor;

searching one or more data structures based on said header data to produce search results using a third peripheral processor;

editing said packet based on said search results, said header data, and said vector using a fourth peripheral processor;

wherein said coordinating comprises,

storing data within a shared register set coupled to each of said peripheral processors,

sharing said data with said parsing, said deconstructing, said searching, and said editing, and

monitoring said deconstructing, said searching, and said editing.

21. **(Canceled)**

22. **(Original)** The computer-readable storage medium of Claim 20, further comprising buffering said packet before said parsing.

23. **(Original)** The computer-readable storage medium of Claim 20, wherein:
said deconstructing further comprises forming a search argument; and
said searching uses said search argument.

24. **(Currently Amended)** A ~~The~~ computer-readable storage medium, comprising computer instructions for ~~of Claim 20, wherein~~:
parsing a packet using a first peripheral processor, said packet having a header portion, to determine a vector;
coordinating processing using said vector;
deconstructing said packet header to form header data using a second peripheral processor;
searching one or more data structures based on said header data to produce search results using a third peripheral processor; and
editing said packet based on said search results, said header data, and said vector using a fourth peripheral processor; wherein
said deconstructing ~~further~~ comprises forming a search argument,[[;]]
said coordinating ~~further~~ comprises,
storing data within a shared register set coupled to each of said peripheral processors,
sharing said data with said parsing, said deconstructing, said searching, and said editing,
monitoring said deconstructing, said searching, and said editing, and
operating on said search argument to form a modified search argument prior to said searching, [[;]] and
said searching uses said modified search argument.

25. **(Previously Presented)** A computer data signal embodied in a carrier wave, comprising computer instructions for:

parsing a packet using a first peripheral processor, said packet having a header portion, to determine a vector;

coordinating processing using said vector;

deconstructing said packet header to form header data using a second peripheral processor;

searching one or more data structures based on said header data to produce search results using a third peripheral processor;

editing said packet based on said search results, said header data, and said vector using a fourth peripheral processor;

wherein said coordinating comprises,

storing data within a shared register set coupled to each of said peripheral processors,

sharing said data with said parsing, said deconstructing, said searching, and said editing, and

monitoring said deconstructing, said searching, and said editing.

26. **(Canceled)**

27. **(Original)** The computer data signal of Claim 25, further comprising buffering said packet before said parsing.

28. **(Original)** The computer data signal of Claim 25, wherein:

said deconstructing further comprises forming a search argument; and

said searching uses said search argument.

29. **(Currently Amended)** A ~~The~~ computer data signal embodied in a carrier wave, comprising computer instructions for ~~of Claim 25, wherein~~:

parsing a packet using a first peripheral processor, said packet having a header portion, to determine a vector;

coordinating processing using said vector;

deconstructing said packet header to form header data using a second peripheral processor;

searching one or more data structures based on said header data to produce search results using a third peripheral processor;

editing said packet based on said search results, said header data, and said vector using a fourth peripheral processor; wherein

said deconstructing ~~further~~ comprises forming a search argument,[[;]]

said coordinating ~~further~~ comprises,

storing data within a shared register set coupled to each of said peripheral processors,

sharing said data with said parsing, said deconstructing, said searching, and said editing,

monitoring said deconstructing, said searching, and said editing, and

operating on said search argument to form a modified search argument prior to said searching,[[;]] and

said searching uses said modified search argument.